Em104-i4231

PC/104 CPU Module

User's Manual

Version 1.0

2009.02

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About User's Manual

This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this User's Manual, please consult your vendor before further handling.

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system.

Replacing the lithium battery

Incorrect replacement of the lithium battery may lead to a risk of explosion. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.
Do not throw lithium batteries into the trashcan. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please consult the user's manual first at:

ftp://ftp.arbor.com.tw/pub/manual

Please do not hesitate to call or e-mail our customer service when you still can not find out the answer.

http://www.arbor.com.tw
E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantibility and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Packing List

1 x Em104-i4231 PC/104 CPU module

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

Ordering Information

Em104-i4231DVL/128M	PC/104 Vortex86SX module with CRT/LCD, LAN and 128M Flash Disk
Em104-i4231DVL/4M	PC/104 Vortex86SX module with CRT/LCD, LAN and 4M SPI Flash Disk
CBK-11-4231-00	Cable Kit USB cable x 2 COM flat cable x 4 IDE flat cable x 1 LPT flat cable x 1 RJ45 cable x 1 VGA cable x 1 KBMS cable x 1

Chapter 1

Introduction

1.1 Specifications

Form Factor	PC/104 CPU module
CPU	DMP Vortex86SX (32-bit x86 Embedded SoC)
Chipset	Integrated in processor (Vortex86SX)
System Memory	128MB DDRII RAM On Board
VGA/ LCD Controller	XGI Z9s w/ 16MB VRAM
Ethernet	1 x 10/100 Base-T Ethernet
BIOS	AMI PnP Flash BIOS
IDE Interface	1 x IDE (UltraATA 33), supports maximum 2 IDE devices • 1 x IDE HDD + 1x NANDFlash disk or • 1 x IDE HDD + 1x CF Disk or • 1 x CF Disk + 1 x NANDFlash disk
Serial Port	4 x Serial Ports (COM3, 4: RS-232, COM1, 2: RS-232/485 selectable)
Parallel Port	1 x SPP/EPP/ECP mode
KBMS	One 1x6 wafer connector for Keyboard and Mouse
Universal Serial Bus	4 x USB 2.0 ports
LCD	18-bit LVDS up to 1280 x 1024 18-bit TTL up to 1280 x 1024
Expansion Interface	1 x CF socket 1 x PC/104
RTC	Real Time Clock
Operation Temp.	-20ºC ~ 70ºC (-4ºF ~ 158ºF)
Watchdog Timer	127-level Reset
Dimension (L x W)	96 x 90 mm (3.8” x 3.5”)

1.2 CPU

The processor is the DMP Votex86SX (SoC - System On Chip) processor, and processor provides the following key features:

- x86 Processor Core
- Embedded I/D Separated L1 Cache
- SDRAM/DDRII Control Interface
- IDE Controller
- LPC (Low Pin Count) Bus Interface
- MAC Controller x 1
- PCI Controller Interface
- ISA Bus Interface
- DMA Controller
- Interrupt Controller
- Counter/ Timers
- MTBF Counter
- Real Time Clock
- FIFO UART Port x 5
- Parallel Port x 1
- General Chip Selector
- General Programmable I/O
- USB 2.0 Host Support
- PS/2 Keyboard and Mouse Interface Support
- Redundant System Support
- Speaker out
- Embedded 256KB Flash
- JTAG Interface supported for S.W. debugging..

1.3 Memory

The board includes 128MB soldered DDR2 SDRAM.

1.4 Ethernet

The board uses the MAC including on CPU for 10/100Mbps Ethernet. Magnetics are included on the board so that complete Ethernet functionality is provided. The PCB layout shall provide the standard Ethernet signal isolation characteristics.

In addition to RJ-45, a 10-pin pin header will be provided with 0 Ohm routing resisters.

Note: the layout must provide for either connector to be isolated without leaving stub traces on the board.

1.5 Standard peripherals

The board provides the following standard system peripherals:

PS/2 ports:	Keyboard and mouse from DMP Vortex86SX chip.
USB ports:	Four USB 2.0 ports from DMP Vortex86SX chip. Minimum 500mA per port drive capability with short circuit / overcurrent protection on each port.
Parallel port:	One parallel connection
IDE port:	One UDMA-33 channel with master/slave support

1.6 Video

The board shall provide an option during development to include a VGA video connector offering support for a CRT. VGA exists inside DMP Vortex86SX. The video controller should idealy be able to share main memory for its frame buffer, but a discrete memory solution will be considered.

1.7 Serial ports

Two ports have RS-232 full 8-signal handshake capability using 115.2kbps transceivers with ESD protection. In some models, COM2 has additional support for RS-422 and RS-485 as well.
All serial port input signals have weak pull-up/down resistors to their inactive state.

1.8 IDE interface

The board contains a standard 44-pin 2mm pitch pin header for connecting up to two IDE devices (Master / Slave) on the channel. The 44-pin connector must be placed so that a cable connected to it may exit the PC/104 board without interfering with the PC/104 mounting holes or any other feature on the board.

1.9 CompacFlash interface

The CF socket is located on the back of the board.
It shares the IDE channel with the solid state storage device.
If compact flash card is inserted it can not exceed the PC/104 outline.

1.10 PC/104 bus expansion

The PC/104 (ISA) bus is provided to enable the mounting of additional I/O boards. The standard configuration shall use stackthrough PC/104 connectors to allow expansion boards to be mounted both above and below the board. Non-stackthrough configuration is also supported as a semi-custom deviation.

1.11 Backup battery

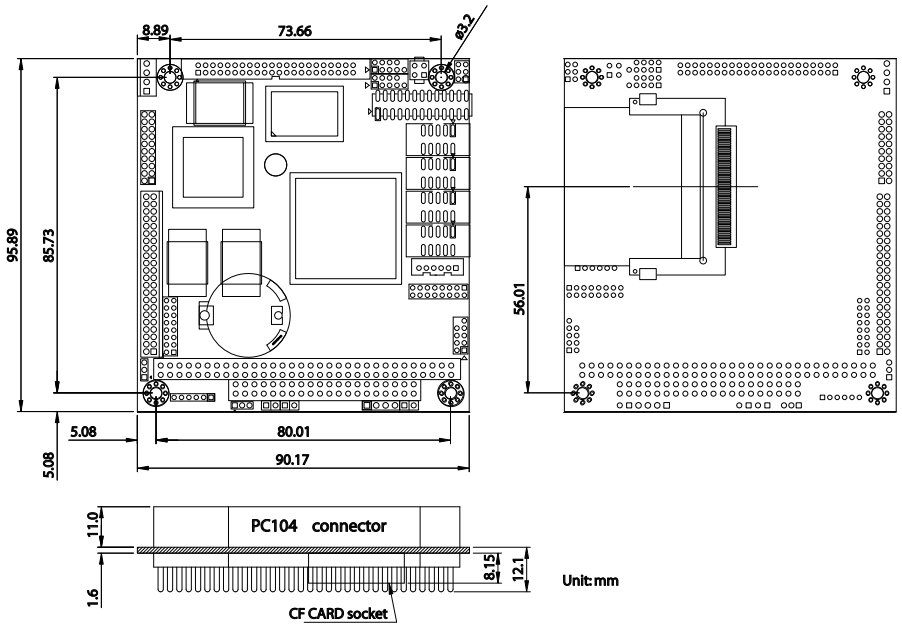
The board includes a backup battery for CMOS RAM and real-time clock backup. The battery is soldered on the top side of the board in an area not underneath the IDE flashdisk.
With a battery current of no more than 2uA, the on board battery life shall be 5 years minimum over the operating temperature range of -40 to +85°C. External battery voltage requirement is 3.3V +/-%10.
The board must be able to boot and function properly without a backup battery installed.

1.12 Power supply

An power connector is provided with +5V and +12V power for use with floppy peripherals.
The board requires +5VDC & +12VDC input voltage. Maximum allowable reflected ripple, measured at the voltage input connector, is 50mV p-p. All switching power supply stages are synchronized to reduce random non-synchronized overlapping spikes.

1.13 Board Dimensions

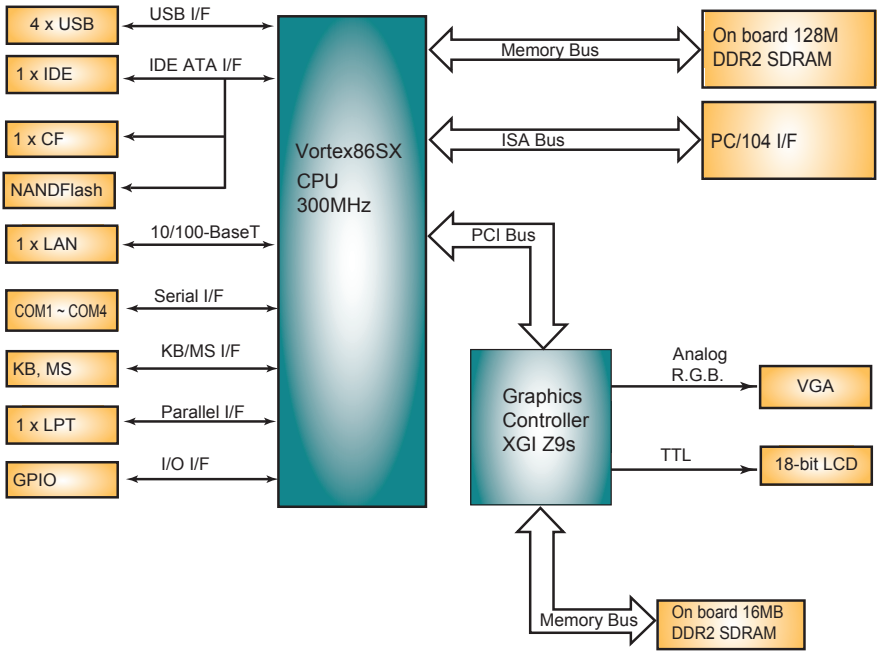
The board outline dimensions are 3.8 ” x 3.5 ” .
Standard stackthrough PC/104 connectors are provided on the board to allow for the addition of PC/104 expansion boards above or below.



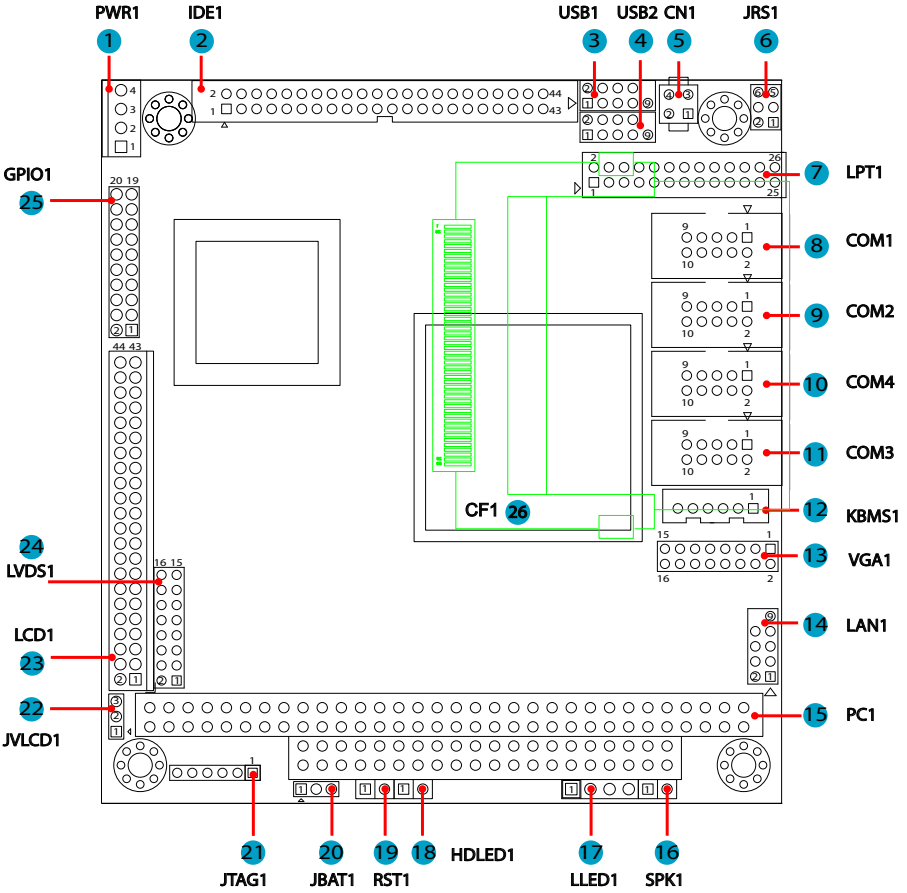
Chapter 2

Installation

2.1 Block Diagrams



2.2 Jumpers and Connectors



Jumpers

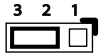
JRS1: COM1, COM2 RS-232/485 Select (6)

It can be configured COM1 and COM2 to operate in RS-232 or RS-485 mode.
Connector type: 2.00mm pitch 2x3-pin headers.

Mode		
RS-232 (Default)	1-3 short 2-4 short	
RS-485	3-5 short 4-6 short	

JBAT1: CLear CMOS Setup (20)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.00 mm pitch 1x3-pin headers.

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated.
Refer to the following solutions to reset your CMOS setting:

Solution A:

1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 1 and pin 2 of JBAT1 for five seconds.
3. Place the shunt back to pin 2 and pin 3 of JBAT1.
4. Power on the system.

Solution B:

If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

Note:

If you are unable to enter BIOS setup, turn the system on and off a few times.

JVLCD1: LCD Panel Voltage Select (22)

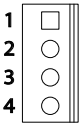
The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.
Connector type: 2.00 mm pitch 1x3-pin headers.

Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	

Connectors

PWR1: Power Supply Connector (1)

Pin	Description
1	+5V
2	GND
3	GND
4	+12V



Connector type: 2.54mm pitch 1x4-pin wafer one wall connector

Input power may be supplied either through this connector, the I/O power connector, or from an external supply or directly through the PC/104 bus power pins if a PC/104 power supply is used with the CPU.

The board requires only +5VDC input power to operate. All other required voltages are generated on board with miniature switching regulators. However since the PC/104 bus includes pins for +5V and ±12V, these voltages may be supplied through this connector if needed.

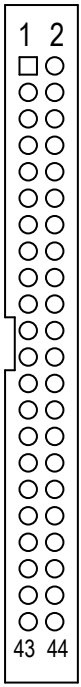
IDE1: Primary IDE Connector (2)

An IDE drive ribbon cable has two connectors to support two IDE devices. If a ribbon cable connects to two IDE drives at the same time, one of them has to be configured as Master and the other has to be configured as Slave by setting the drive select jumpers on the drive.

Consult the documentation that came with your IDE drive for details on jumper locations and settings. You must orient the cable connector so that the pin 1 (color) edge of the cable corresponds to pin 1 of the IDE connector.

Connector type: 2.0mm pitch 2x22-pin box headers.

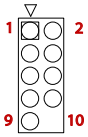
Pin	Description	Pin	Description
1	RESET#	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	N/C
21	DREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IRDY	28	GND
29	ACK#	30	GND
31	IRQ	32	N/C
33	AD1	34	ATA66 DETECT
35	AD0	36	AD2
37	CS#0	38	CS#1
39	ACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C



USB1, USB2: USB Connectors (3,4)

USB1 supports two USB 2.0 w/ 480MB/s by pin headers

Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	GND	10	N/C (Key)



Connector type: 2.00mm pitch 2x5-pin headers

CN1: RS-485 Output Connector (5)

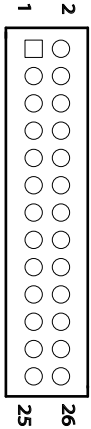
Connector type: 2.54mm pitch 2x2-pin headers.

Pin	Description	Pin	Description
1	1-RS-485+	2	1-RS-485-
3	2-RS-485+	4	2-RS-485-

LPT1: Parallel Port Connector (7)

Connector type: 2.0mm pitch 2x13-pin headers.

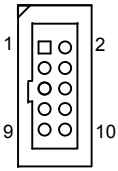
Pin	Description	Pin	Description
1	STB#	2	AFD#
3	PTD0	4	ERROR#
5	PTD1	6	INIT#
7	PTD2	8	SLIN#
9	PTD3	10	GND
11	PTD4	12	GND
13	PTD5	14	GND
15	PTD6	16	GND
17	PTD7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	GND



COM1~4: Serial Port Connectors (8, 9, 10, 11)

COM3, COM4: RS-232; COM1, COM2: RS-232/485 selectable.
Connector type: 2.00mm pitch 2x5-pin box headers.

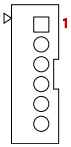
Pin	Description	Pin	Description
1	DCD#	2	RXD
3	TXD	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C



KBMS1: Keyboard & Mouse Connector (12)

Connector type: 2.00mm pitch 1x6-pin wafer connector

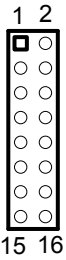
Pin	Description
1	KB_DATA
2	GND
3	MS_DATA
4	KB_CLK
5	PS2_VCC
6	MS_CLK



VGA1: CRT Connector (13)

Connector type: 2.00mm pitch 2x8-pin headers.

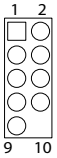
Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	N/C
5	GND	6	GND
7	GND	8	GND
9	CRT VCC5	10	N/C
11	N/C	12	VDDAT
13	HSYNC	14	VSYNC
15	VDCLK	16	N/C



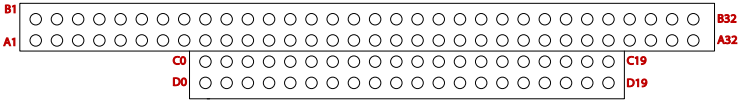
LAN1: Ethernet Connector (14)

Connector type: 2.00mm pitch 2x5-pin headers.

Pin	Description	Pin	Description
1	TX+	2	TX-
3	RX+	4	N/C
5	N/C	6	RX-
7	N/C	8	N/C
9	GND	10	N/C (Key)



PC1: PC/104 ISA Interface (15)



PC1 provides a standard PC/104 16-bit ISA bus. The connectors may be either soldered-in or press-fit versions. The standard configuration provides stackthrough connectors enabling I/O boards to be mounted both above and below the board. In custom configurations the board is available with non-stackthrough connectors enabling only top-side I/O board installation.

The PCB holes must be designed with the appropriate hole dimensions and plating thickness to support the reliable use of press-fit connectors in addition to hand-soldered connectors. For cost reduction, hand-soldered connectors may be used as long as the soldering meets IPC 610 class 2 standards.

On PC1, the Key pins are cut on the bottom of the connector and plugged on top.

Pin	Description	Pin	Description	Pin	Description	Pin	Description
D0	GND	C0	GND	A1	IOCHCK#	B1	GND
D1	MEMCS16#	C1	SBHE#	A2	SD7	B2	RST_DRV
D2	IOCS16#	C2	LA23	A3	SD6	B3	+5V
D3	IRQ10	C3	LA22	A4	SD5	B4	IRQ9
D4	IRQ11	C4	LA21	A5	SD4	B5	N/C
D5	IRQ12	C5	LA20	A6	SD3	B6	DREQ2
D6	IRQ15	C6	LA19	A7	SD2	B7	N/C
D7	IRQ14	C7	LA18	A8	SD1	B8	0WS#
D8	DACK0#	C8	LA17	A9	SD0	B9	+12V
D9	DREQ0	C9	MEMR#	A10	IOCHRDY	B10	GND
D10	DACK5#	C10	MEMW#	A11	AEN	B11	SMEMW#
D11	DREQ5	C11	SD8	A12	SA19	B12	SMEMR#
D12	DACK6#	C12	SD9	A13	SA18	B13	IOW#
D13	DREQ6	C13	SD10	A14	SA17	B14	IOR#
D14	DACK7#	C14	SD11	A15	SA16	B15	DACK3#
D15	DREQ7	C15	SD12	A16	SA15	B16	DREQ3
D16	+5V	C16	SD13	A17	SA14	B17	DACK1#
D17	MASTER#	C17	SD14	A18	SA13	B18	DREQ1
D18	GND	C18	SD15	A19	SA12	B19	REFRESH#
D19	GND	C19	GND	A20	SA11	B20	SYSCLK
				A21	SA10	B21	IRQ7
				A22	SA9	B22	IRQ6
				A23	SA8	B23	IRQ5
				A24	SA7	B24	IRQ4
				A25	SA6	B25	IRQ3
				A26	SA5	B26	DACK2#
				A27	SA4	B27	TC
				A28	SA3	B28	BALE
				A29	SA2	B29	+5V
				A30	SA1	B30	ISA_CLK
				A31	SA0	B31	GND
				A32	GND	B32	GND

Connector type: PC104 PRESS FIT 2x20P connector

SPK1: Speaker Connector (16)

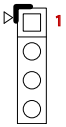
Connector type: 2.54mm pitch 1x2-pin headers.

Pin	Description
1	SPEKOUT+
2	SPEKOUT-

LLED1: LAN LED indicators (17)

Connector type: 2.54mm pitch 1x4-pin headers.

Pin	Description
1	LINK_LED+
2	LINK_LED-
3	ACT_LED+
4	ACT_LED-



HDLED1: HDD LED Connector (18)

Connector type: 2.54mm pitch 1x2-pin headers.

Pin	Description
1	HDD_LED-
2	HDD_LED+

RST1: Reset Connector (19)

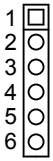
Connector type: 2.54mm pitch 1x2-pin headers.

Pin	Description
1	RESET-
2	RESET+

JTAG1: JTAG connector (21)

Connector type: 2.00mm pitch 1x6-pin headers.

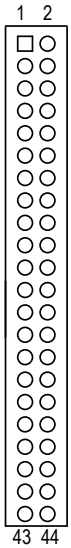
Pin	Description
1	+5V
2	TCK
3	TDO
4	TDI
5	TMS
6	GND



LCD1: LCD Connector (23)

Connector type: 2.00mm pitch 2x22-pin headers.

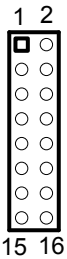
Pin	Description	Pin	Description
1	VLCD	2	VLCD
3	G2	4	G3
5	G4	6	G5
7	N/C	8	N/C
9	R0	10	R1
11	R2	12	R3
13	R4	14	R5
15	GND	16	N/C
17	N/C	18	N/C
19	N/C	20	GND
21	N/C	22	N/C
23	B0	24	B1
25	B2	26	B3
27	B4	28	B5
29	N/C	30	N/C
31	G0	32	G1
33	GND	34	GND
35	N/C	36	CLOCK
37	N/C	38	DE
39	N/C	40	HSYNC
41	N/C	42	VSYNC
43	BACK_L	44	VDDEN



LVDS1: LVDS Connector (24)

Connector type: 2.00mm pitch 2x8-pin headers.

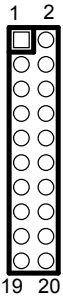
Pin	Description	Pin	Description
1	LCD_VCC	2	LCD_VCC
3	GND	4	GND
5	L0+	6	L0-
7	L1-	8	GND
9	GND	10	L1+
11	L2+	12	L2-
13	CLOCK-	14	GND
15	GND	16	CLOCK+



GPIO1: Digital I/O Connector (25)

Supports 16-bit GPIO, the signals can be programmable by user define.
Connector type: 2.00mm pitch 2x10-pin headers.

Pin	Description	Pin	Description
1	GND	2	+5V
3	GP0	4	GP8
5	GP1	6	GP9
7	GP2	8	GP10
9	GP3	10	GP11
11	GP4	12	GP12
13	GP5	14	GP13
15	GP6	16	GP14
17	GP7	18	GP15
19	+5V	20	GND

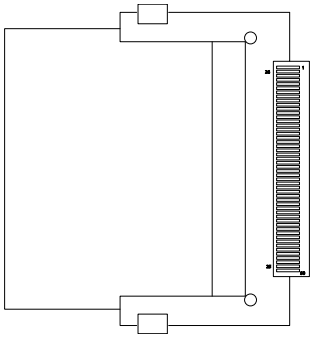


CF1: CompactFlash Socket (26)

Compact Flash (CF) card is “not hot-swap”. If the CF card is swapped in the condition of system power-on, it will damage the CF card.

1. Make sure the Single Board Computer is powered OFF.
2. Plug the Compact Flash Type II device into its socket. Verify the direction is correct.
3. Power up the system.

Pin	Description	Pin	Description
1	GND	26	GND
2	SDD3	27	SDD11
3	SDD4	28	SDD12
4	SDD5	29	SDD13
5	SDD6	30	SDD14
6	SDD7	31	SDD15
7	SDCS0#	32	SDCS1#
8	GND	33	GND
9	GND	34	SDIOR#
10	GND	35	SDIOW#
11	GND	36	+5V
12	GND	37	SIDEIRQ
13	+5V	38	+5V
14	GND	39	CSEL#
15	GND	40	N/C
16	GND	41	SIDERST#
17	GND	42	SIORDY
18	SDA2	43	SDDREQ
19	SDA1	44	SDDACK#
20	SDA0	45	HD_LED2#
21	SDD0	46	SDIAG#
22	SDD1	47	SDD8
23	SDD2	48	SDD9
24	N/C	49	SDD10
25	GND	50	GND



2.3 The Installation Paths of CD Driver

Driver	Path
Ethernet	\Ethernet\RDCR6040\LINUX_2422 \Ethernet\RDCR6040\DOS_070419
VGA	\GRAPHICS\XGI\

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Chapter 3

Driver Installation

3.1 DOS driver installation

For Vortex86SX with 100M LAN, you should use R6040 packet driver.

```
C:\DSOCK\DEMO\EXE>r6040pd 0x62
```

where software interrupt 62H can be any number between 60H and 70H. Or run pktdrv4.bat in directory “EXE” to load packet driver:

```
C:\DSOCK\DEMO\EXE>pktdrv (Load packet driver for Vortex86SX)
C:\DSOCK\DEMO\EXE>ftpd (Run any DSock example program)
```

Note:

The default setting of network is on DSOCK.CFG. You should modified the default setup upon your network. After changing the DSOCK.CFG, you can run examples.

DSOCK.CFG

DSOCK.CFG is a text file to save network information for DSock. There are two way for DSock to get network setup:

BOOT/DHCP or DSOCK.CFG. Call DSock_DoBootp() to use BOOT/DHCP protocol to get network setting when BOOT / DHCP servers exist. Or write network setting into DSOCK.CFG that DSock will read setting form it. Use DSOCK.CFG can guarantee IP address is fixed. There are four main statement of DSOCK.CFG: ip, netmask, gateway, nameserver, Typical setup of DSOCK.CFG:

```
ip=192.168.0.234
netmask=255.255.255.0
gateway=192.168.0.1
nameserver=192.168.0.1
```

If you have no DNS server, you can do this: "nameserver=". If you have no gateway, the same way as nameserver tag.

Packet Driver

Because of DSock is designed for M6117D which is a 386 SX CPU, Realtek 8019AS chip will used by M6117D series. The default IRQ is set to 5 and I/O address is 320H. So just add those into your autoexec.bat:

```
ne2000 0x62 5 0x320
```

3.2 Linux driver installation

This section we will concentrate discussion on kernel 2.6.18. We suppose that you have prior experience of kernel compiling. You should already know how to configure and compile the Linux kernel. If not, we suggest that you might read some Linux kernel compiling articles before you proceed.
Here is a package which contains a config file and an essential patch file for Linux kernel 2.6.118. Please copy the config file to the kernel directory and apply the patch. Finally, run “make menuconfig“ to be ready to configure your Linux kernel.

```
(Go to your kernel source directory)
# cd/usr/src/linux-2.6.18-DMP

(Extract files from our package)
# tar -xzvf xxx.tar.gz

(Copy the configuration file to overwrite .config)
# cp -a xxx.config .config

(Apply the patch file)
# patch -p1 < xxx.patch

(Configure the Linux kernel with  a ncurses-based tool)
# make menuconfig
```

CPU

Vortex86SX integrates the RISC core that contains all the features of the 486SX microprocessor, and the instruction set of Vortex86SX is compatible with 486 as well, so please directly select 486 as the processor family in the Linux kernel setting.

```
Processor type and features --->
Subarchitecture Type (PC-compatible) --->
Processor family (486) --->
(For generic optimizations)
[*] Generic x86 support
```

Vortex86SX doesn't have the math coprocessor, so you have to enable the math emulation of the Linux kernel.

IDE

The IDE controller can be configured as the native or the legacy mode in BIOS setting. The default setting is the legacy mode, if you do not alter it, the IDE controller should work fine in most cases except for the IDE DMA mode.

If you have good reasons to switch the default setting to the native mode, you need an IT821X driver with a patch for Linux kernel 2.6.18, even if you did not need the DMA support.

However, no matter which mode you choose, if the DMA mode is required, you need the IT821X driver with our patch and selecting the following options on the kernel configuration menu to enable the DMA support.

```
Device Drivers --->
ATA/ATAPI/MFM/RLL support --->
<*> ATA/ATAPI/MFM/RLL support
<*> Enhanced IDE/MFM/RLL disk/cdrom/tape/floppy support
<*> Include IDE/ATA-2 DISK support
<*> generic/default IDE chipset support
[*] PCI IDE chipset support
[*] Sharing PCI IDE interrupts support
[*] Generic PCI bus-master DMA support
[*] Use PCI DMA by default when available
<*> IT821X IDE support
```

By the way, you cannot use the IDE DMA as well as the native mode under Linux kernel 2.4, because there is no available driver.

```
Device Drivers --->
    ATA/ATAPI/MFM/RLL support --->
      <*> ATA/ATAPI/MFM/RLL support
      <*> Enhanced IDE/MFM/RLL disk/cdrom/tape/floppy support
      <*> Include IDE/ATA-2 DISK support
      <*> generic/default IDE chipset support
```

Note:

The controller supports Ultra-DMA, but at the present time there are some problems of it, so that you will probably encounter a system error when you try to boot from the storage device which support the UDMA mode. For the problem, we have modified the IDE driver to force all UDMA modes to be downgraded to the MDMA2 mode.

Networking

Vortex86SX contains a R6040 network function. It is a 10/100M Fast-Ethernet controller and it provides full compliance with IEEE 802.3u 100 Base-T specifications and IEEE 802.3x full duplex flow control.

Currently, there is no available driver in the Linux kernel.

Therefore, before you configure the kernel, you should already patch the kernel for the device driver. Then, please select the R6040 support, and enable NAPI if you need it.

```
        (R6040 need PCI support)
        Bus options (PCI, PCMCIA, EISA, MCA, ISA) --->
            [*] PCI support
        Device Drivers --->
        Network device support --->
            [*] Network device support
...
        Ethernet (10 or 100Mbit) --->
            [*] Ethernet (10 or 100Mbit)
...
            [*] EISA, VLB, PCI and on board controllers
                <*> RDC R6040 PCI Fast Ethernet support
                (If needed)
                [*] Use Rx Polling (NAPI)
```

Display

XGI Z9s is the graphics controller on the Vortex86SX evaluation board, VSX-6190. It is designed to provide essential functions for embedded applications; moreover, it is easy to be configured under GNU/Linux.
XGI Z9s can work well with native SiS/XGI driver under the Linux kernel or the X Window System. For the frame buffer support of Linux, please enable the following options in the kernel configuration menu.

```
Device Drivers --->
  Graphics support --->
      <*> Support for frame buffer devices
          <*> SiS/XGI display support
          [*] SiS 315/330/340 series and XGI support
...
      Console display driver support --->
          <*> Framebuffer Console support
```

For the X Window System support, there are three things need to be dealt with.

First, you can use X11R6.8 or higher version, which the internal driver in can work properly. Or the other versions with a modified driver by Dr. Thomas Winischhofer, download it from http://www.winischhofer.eu/linuxsisvga.shtml.

Second, we suggest not using X11R7.2, because there is a bug which lead to X server fails to start up, when the X server was enabled MMX checking and CPU didn't support the CPUID instruction.

Third, you should place a driver option in device section of your configuration file:

```
Section "Device"
  Driver "sis"
  Option "BenchmarkMemcpy" "no"
...
EndSection
```

It avoids a system error when X server is starting up.

USB

Vortex86SX contains one EHCI host controller and one OHCI host controller, so you need to enable these options:

```
Device Drivers --->
    USB support --->
        <*> Support for Host-side USB
        [*] USB device filesystem
        <*> EHCI HCD (USB 2.0) support
        <*> OHCI HCD support
```

Then, add the following line in your /etc/fstab file.

```
none /proc/bus/usb usbfs defaults 0 0
```

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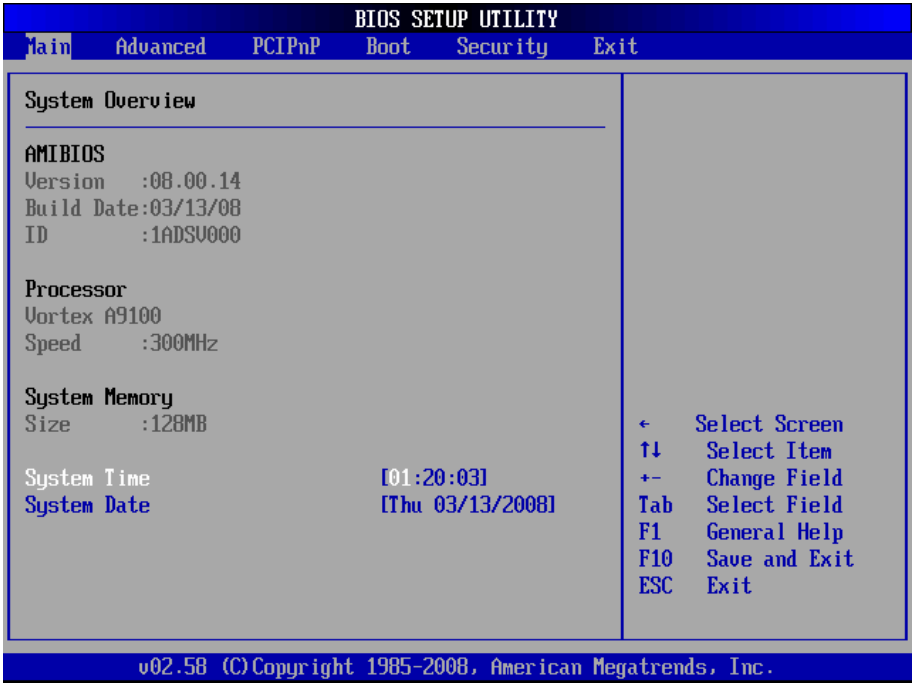
Chapter 4

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility.

When you turn on the computer, the AMI BIOS is immediately activated. The Main allows you to select several configuration options. Use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.



Processor

This part shows the auto-detected CPU specification.
DM&P Semiconductor is the Vortex86SX 32-Bit Microprocessor, DDR2 128MB onboard, which is based on x86 structure. It is the x86 SoC (System on Chip) with 0.13 micron process and ultra low power consumption design (less than 1 watt). The CPU on the Vortex86SX is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based,
Linux and most popular 32-bit RTOS.

System Memory

This part shows the auto-detected system memory.
The Vortex86SX is a high performance with 128MB RAM and speed 133MHz onboard and fully static 32-bit x86 processor, which is compatible with DOS and Linux. It integrates 32KB write through direct map L1 cache, PCI Rev. 2.1 32-bit bus interface at 33MHz, SDRAM, DDR2, ROM controller. IPC (Internal Peripheral Controllers with DMA and interrup timer/ counter included), Fast Ethernet MAC, FIFO UART, USB 2.0 Host and IDE controller into a System-on-Chip (SoC) design.
The Vortex86SX are all 128MB onboard and the speed is 133MHz.

System Time

Set the system time.
The time format is:

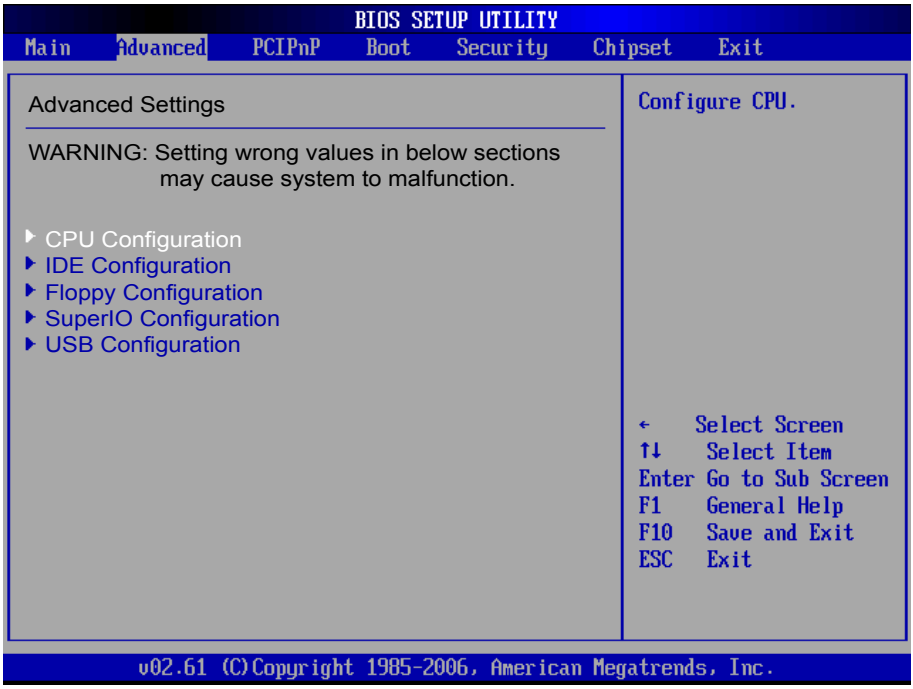
Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.
The date format is:

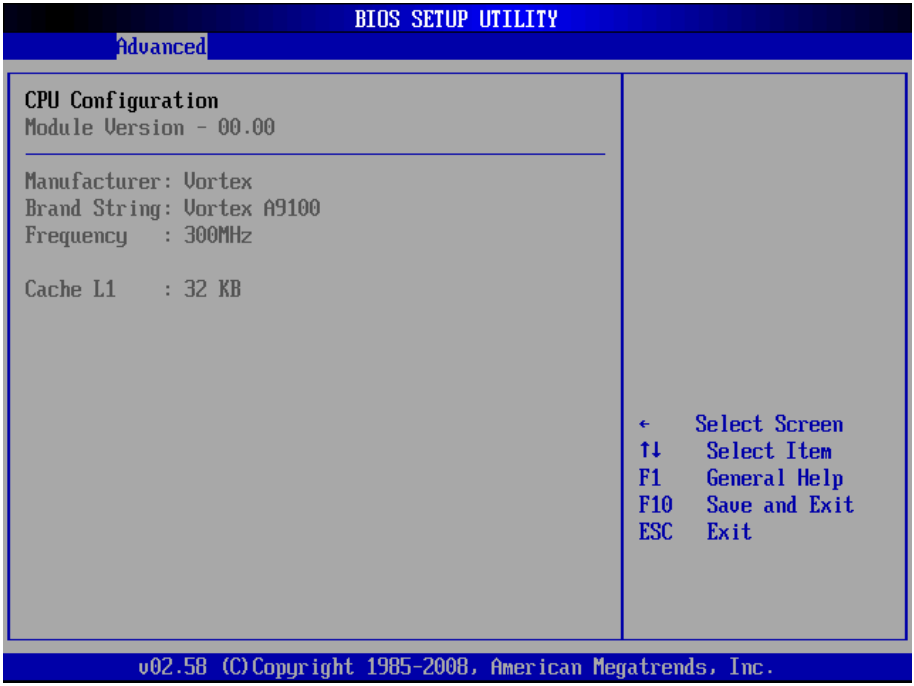
Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

3.2 Advanced Settings

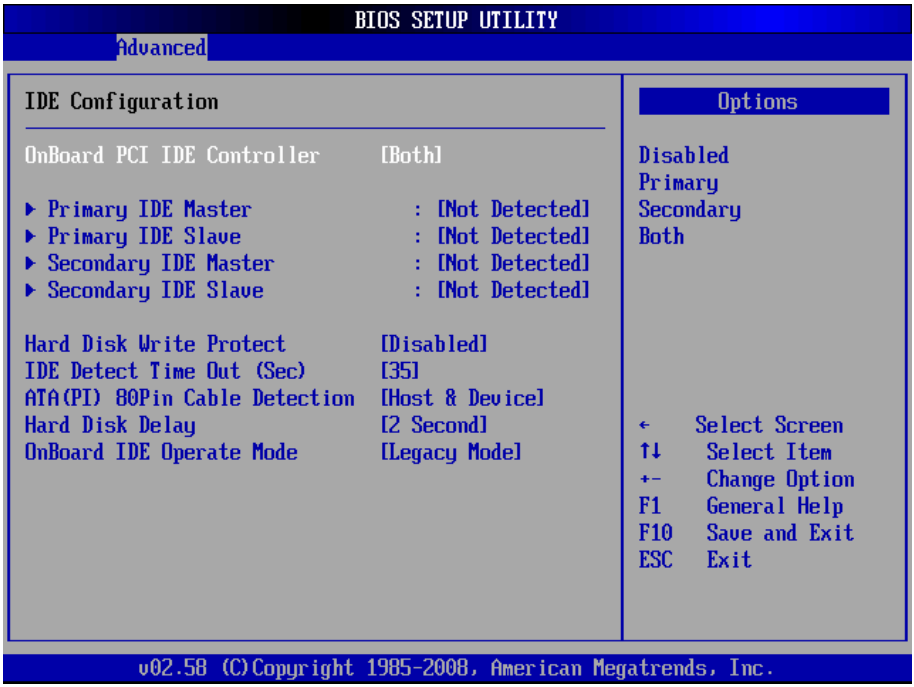


3.2.1 CPU Configuration

This will show the CPU related information detected by BIOS.



3.2.2 IDE Configuration



OnBoard PCI IDE Controller

This can select the specification you wanted for the IDE device.
This option specifies the channel used by IDE controller on the motherboard.

Option	Description
Disabled	Set this value to prevent the computer system from using the onboard IDE controller.
Primary	Set this value to allow the computer system to detect only Primary IDE channel. This includes both the Primary Master and the Primary Slave.
Secondary	Set this value to allow the computer system to detect only Secondary IDE channel. This includes both the Secondary Master and the Secondary Slave.
Both (Default)	Set this value to allow the computer system to detect Primary and Secondary IDE channels. This includes both the Primary Master, Primary Slave, Secondary Master and the Secondary Slave.

Primary and Secondary IDE Master/Slave

When you entered the IDE devices, the BIOS will auto-detected and show the detail information of IDE devices.
If you want to change with the IDE configuration, select the item and press the <Enter> to configure the item you wanted.
Select the type of IDE drive. Setting to Auto allows automatic selection of the appropriate IDE device type. Select CDROM if you are specifically configuring a CD-ROM drive. Select ARMD (ATAPI Removable Media Device) if your device is either a ZIP, LS-120 or MO drive.
Configuration options: [Not Installed], [Auto], [CDROM], [ARMD]

Option	Description
Not Installed	Set this value to prevent the BIOS from searching for an IDE disk drive on the specified channel
Auto (Default)	Set this value to allow the BIOS auto detect the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel.
CDROM	This option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS will not attempt to search for other types of IDE disk drives on the specified channel.
ARMD	This option specifies an ATAPI Removable Media Device. This includes, but is not limited to: ZIP, LS-120

Hard Disk Write Protect

This will allow you to enable or disable the hard disk write protection and this will only effective if you configure your device through BIOS.

Option	Description
Disabled (Default)	Set this value to allow the hard disk drive to be used normally. Read, write, and erase functions can be performed to the hard disk drive
Enabled	Set this value to prevent the hard disk drive from being erased.

IDE Detect Time Out (Sec)

Select the time out value for detecting IDE devices.
Configuration options: [0], [5], [10], [15], [20], [25], [30], [35]

Option	Description
0	This value is the best setting to use if the onboard IDE controllers are set to a specific IDE disk drive in the AMIBIOS.
5	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in five seconds. A large majority of ultra ATA hard disk drives can be detected well within five seconds.
10	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 10 seconds.
15	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 15 seconds.
20	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 20 seconds.
25	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 25 seconds.
30	Set this value to stop the AMIBIOS from searching the IDE bus for IDE disk drives in 30 seconds.
35 (Default)	It is the recommended setting when all IDE connectors are set to AUTO in the AMIBIOS setting.

ATA (PI) 80 pin Cable Detection

Set this option to select the method used to detect the ATA (PI) 80 pin cable. The Optimal and Fail-safe setting is Host & Device.

Option	Description
Host & Device (Default)	Set this value to use both the motherboard onboard IDE controller and IDE disk drive to detect the type of IDE cable used.
Host	Set this value to use mother board onboard IDE controller to detect the type of IDE cable used.
Device	Set this value to use IDE disk drive to detect the type of IDE cable used.

The use of an 80-conductor ATA cable is mandatory for running Ultra ATA/66, Ultra ATA/100 and Ultra ATA/133 IDE hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.
80-conductor ATA cable is plug compatible with the standard 40-conductor ATA cable.
Because of this, the system must determine the presence of the correct cable. This detection is achieved by having a break in one of the lines on the 80-conductor ATA cable that is normally an unbroken connection in the standard 40-conductor ATA cable. It is this break that normally an unbroken connection in the standard 40-conductor ATA cable. It is this break that is used to make this determination. The AMIBIOS can instruct the drive to run at the correct speed for the cable type detected.

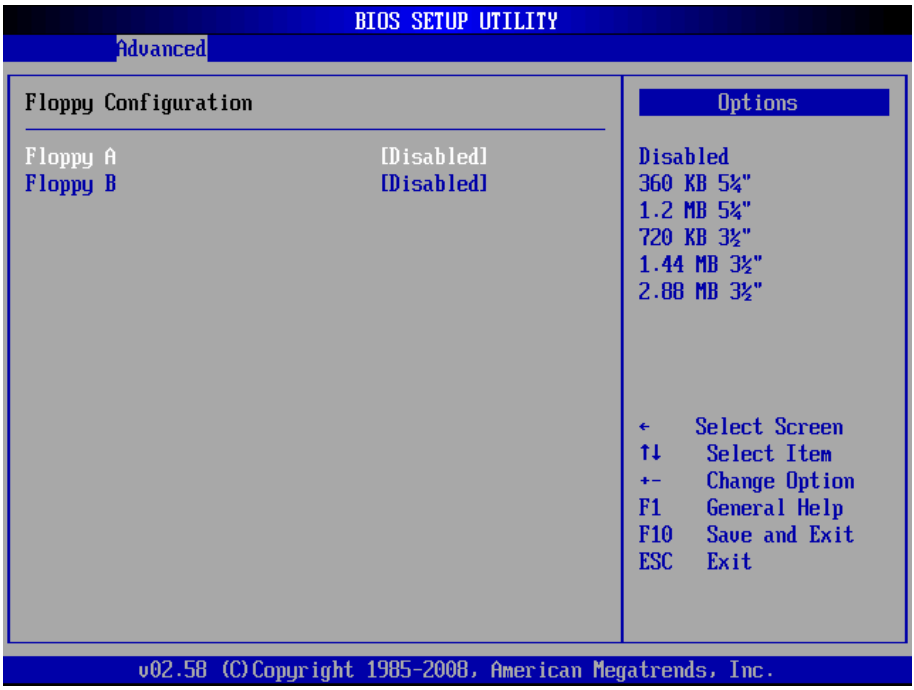
Hard Disk Delay

Delay for a connected HDD (secs). The length of time in seconds the BIOS will wait for a hard disk to be ready for operation. If the hard drive is not ready, the BIOS might not detect the hard drive correctly. The range is from 0~8 seconds.
We suggest the delay time select 2 sec.

OnBoard IDE Operate Mode

The items in this menu Allows you to set or change the configurations for the IDE devices installed in the system. Select an item then press “Enter“ if you want to configure the item.

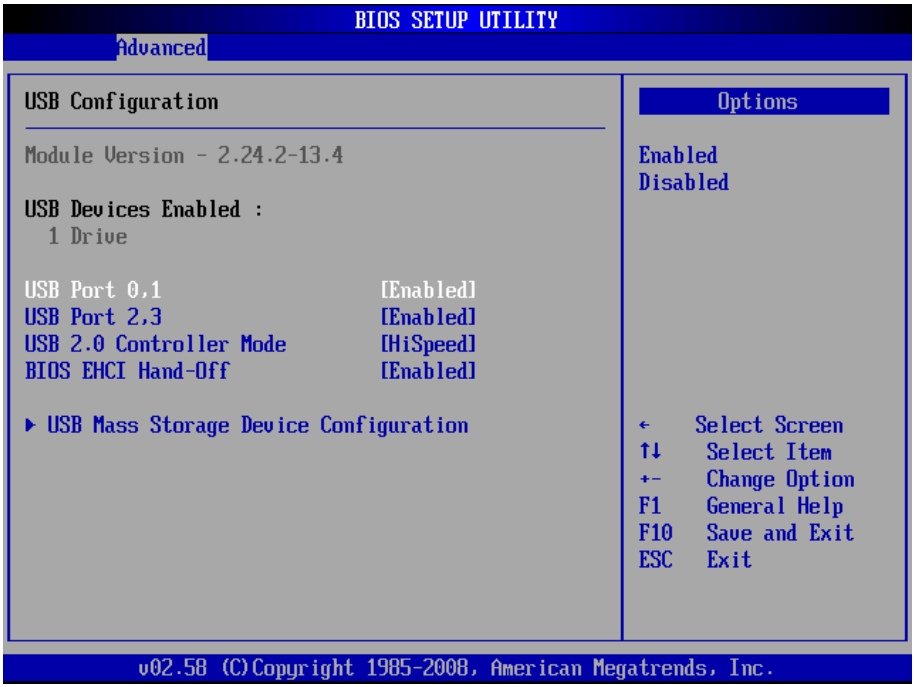
3.2.3 Floppy Configuration



Select the type of floppy disk drive installed in your system.
Configuration options:

Disabled: No diskette drive installed
360K 5.25”
1.2M 5.25”
720K 3.5”
1.44M 3.5”
2.88M 3.5”

3.2.4 USB Configuration



USB 2.0 Controller Mode

Configures the USB 2.0 controller in High Speed (480Mbps) or Full Speed (12MBPS).

BIOS EHCI Hand-Off

This is a work around for OSs without EHCI hand-Off support. The EHCI ownership change should claim by EHCI driver.

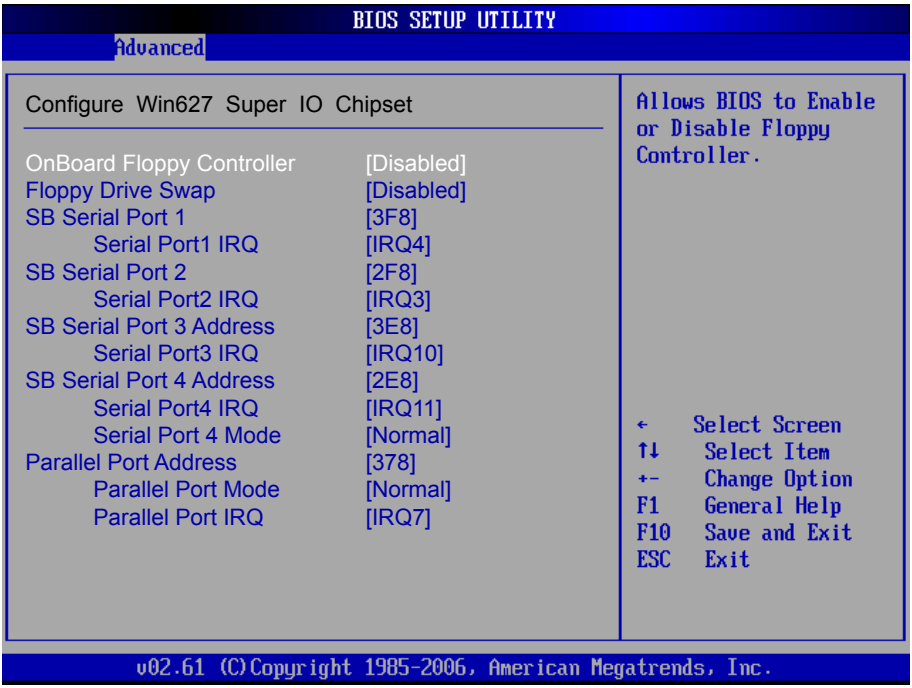
USB Mass Storage Reset Delay

Number of seconds POST waits for the USB mass storage device after start unit command.

Emulation Type

If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to BOOT as FDD. (Ex. ZIP drive).

3.2.5 Super IO Configuration


BIOS SETUP UTILITY
Advanced
Configure Win627 Super IO Chipset
OnBoard Floppy Controller [Disabled]
Floppy Drive Swap [Disabled]
SB Serial Port 1 [3F8]
Serial Port1 IRQ [IRQ4]
SB Serial Port 2 [2F8]
Serial Port2 IRQ [IRQ3]
SB Serial Port 3 Address [3E8]
Serial Port3 IRQ [IRQ10]
SB Serial Port 4 Address [2E8]
Serial Port4 IRQ [IRQ11]
Serial Port 4 Mode [Normal]
Parallel Port Address [378]
Parallel Port Mode [Normal]
Parallel Port IRQ [IRQ7]
Allows BIOS to Enable or Disable Floppy Controller.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

Onboard Floppy Controller

Select “Enabled” if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.

Configuration options: [Enabled], [Disabled]

Floppy Drive Swap

This option allows you to Enabled or Disabled the Floppy Drive Swap.

Configuration options: [Enabled], [Disabled]

Serial Port1 / Port2 Address

Select an address and corresponding interrupt for the first and second serial ports.

Configuration options: [3F8/IRQ4], [2E8/IRQ3], [3E8/IRQ4], [2F8/IRQ3], [Disabled], [Auto]

Parallel Port Address

Select an address for the parallel port.

Configuration options: [Disabled], [3BC], [378], [278]

Option	Description
Disabled	Set this value to prevent the parallel port from accessing any system resources. When the value of this option is set to Disabled, the printer port becomes unavailable.
378	Set this value to allow the parallel port to use 378h as its I/O port address. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O port 378h as the standard setting.
278	Set this value to allow the parallel port to use 278h as its I/O port address.
3BC	Set this value to allow the parallel port to use 3BCh as its I/O port address.

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select Normal, Compatible or SPP unless you are certain your hardware and software both support one of the other available modes.
Configuration options: [Bi-Directional], [EPP], [ECP], [Normal], [Disabled]

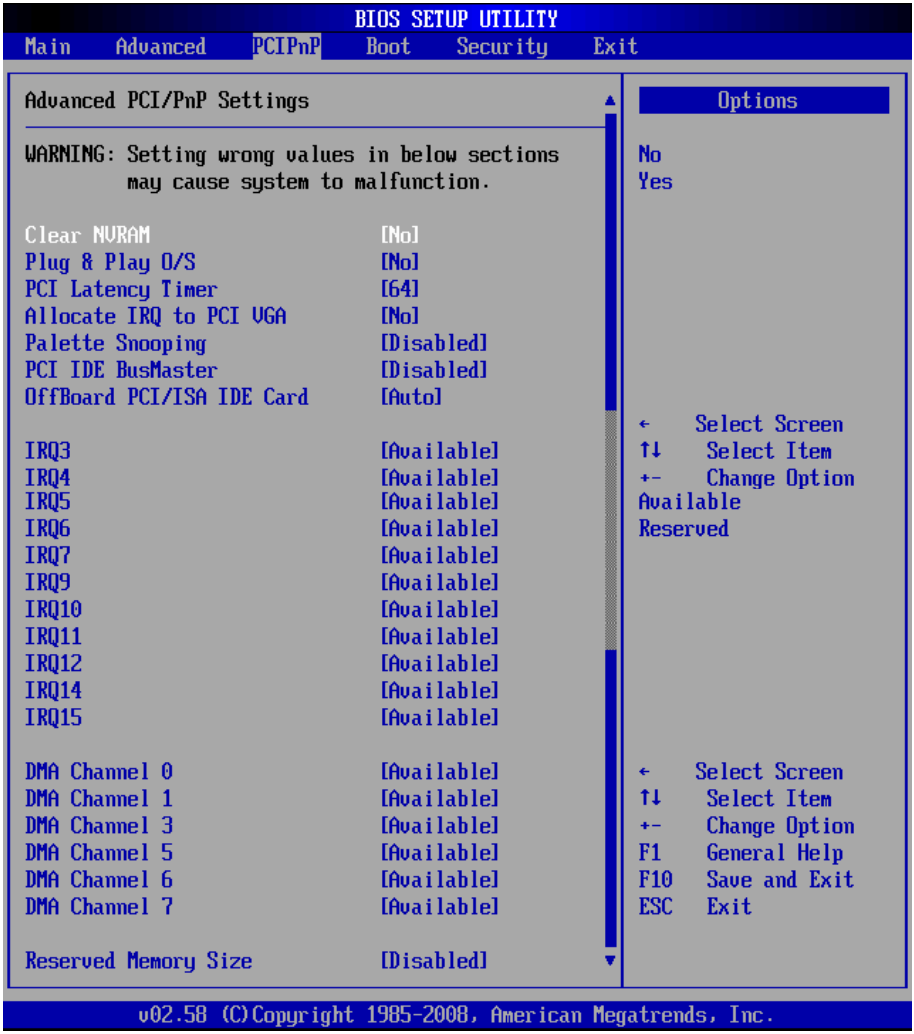
Option	Description
Normal (Default)	Set this value to allow the standard parallel port mode to be used.
Bi-Directional	Set this value to allow data to be sent to and received from the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Mb per second. ECP provides symmetric bi-directional communication.

Parallel Port IRQ

Select an interrupt for the parallel port.
Configuration options: [IRQ5], [IRQ7]

Option	Description
5	Set this value to allow the parallel port to use Interrupt 5.
7 (Default)	Set this value to allow the parallel port to use Interrupt 7. The majority of parallel ports on computer system use IRQ7 and I/O port 378h as the standard setting.

3.3 Advanced PCI/PnP Settings



Clear NVRAM

Clear NVRAM during System BOOT.

Configuration options: Yes, No.

Plug & Play O/S

Set this value to allow the system to modify the settings for Plug and Play operating system support.

Option	Description
No (Default)	The No setting is for operating system that do not meet the Plug and Play specifications. It allows the BIOS to configure all the devices in the system
Yes	The Yes setting allows the operating system to change the interrupt, I/O and DMA setting. Set this option if the system is running Plug and Play aware operating systems.

PCI Latency Timer

Value in units of PCI clocks for PCI device latency timer register.
Configuration option: 32, 64, 96, 128, 160, 192, 224, 248

Option	Description
32	This option sets the PCI latency to 32 PCI clock cycles.
64 (Default)	This option sets the PCI latency to 64 PCI clock cycles.
96	This option sets the PCI latency to 96 PCI clock cycles.
128	This option sets the PCI latency to 128 PCI clock cycles.
160	This option sets the PCI latency to 160 PCI clock cycles.
192	This option sets the PCI latency to 192 PCI clock cycles.
224	This option sets the PCI latency to 224 PCI clock cycles.
248	This option sets the PCI latency to 248 PCI clock cycles.

This options sets the latency of all PCI devices on the PCI bus. This decides how long a PCI device can hog the PCI bus for, higher setting, hogs the bus a little longer, lower setting lets go quicker but stuff like some PCI sound cards will start to crackle.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

Option	Description
Yes (Default)	Set this value to allow the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.
No	Set this value to prevent the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.

Palette Snooping

When set to “Enabled“, the palette snooping feature informs the PCI devices that an ISA graphics device is installed in the system so that the latter can function correctly.
Configuration options: [Disabled], [Enabled].

Option	Description
Disabled (Default)	This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.
Enabled	This setting informs the PCI devices that an ISA based Graphics device is installed in the system. it does this so the ISA based Graphics card will function correctly. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card’s manuals first, be modifying the default setting in the BIOS.

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE busmastering.
Configuration options: [Disabled], [Enabled].

Option	Description
Disabled (Default)	Set this value to prevent PCI busmastering.
Enabled	This option specifies that the IDE controller on the PCI local bus has mastering capabilities.

OffBoard PCI/ISA IDE Card

Set this value to allow the OffBoard PCI/ISA IDE Card to be selected.
Configuration options: [Auto], [PCI Slot1], [PCI Slot2], [PCI Slot3], [PCI Slot4], [PCI Slot5], [PCI Slot6]

Option	Description
Auto (Default)	This setting will auto select the location of an OffBoard PCI IDE adapter card.
PCI Slot1	This setting will select PCI Slot 1 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 1.
PCI Slot2	This setting will select PCI Slot 2 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 2.
PCI Slot3	This setting will select PCI Slot 3 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 3. This option is available even if the mother board does not have a PCI Slot 3. If the mother board does not have a PCI Slot 3, do not use this setting.
PCI Slot4	This setting will select PCI Slot 4 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 4. This option is available even if the mother board does not have a PCI Slot 4. If the mother board does not have a PCI Slot 4, do not use this setting.
PCI Slot5	This setting will select PCI Slot 5 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 5. This option is available even if the mother board does not have a PCI Slot 5. If the mother board does not have a PCI Slot 5, do not use this setting.
PCI Slot6	This setting will select PCI Slot 6 as the location of the OffBoard PCI IDE adapter card. Use this setting only if there is an IDE adapter card installed in PCI Slot 6. This option is available even if the mother board does not have a PCI Slot 6. If the mother board does not have a PCI Slot 6, do not use this setting.

IRQ3 - IRQ15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for use by Legacy ISA devices.

Interrupt	Option	Description
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ14 IRQ15	Available (Default)	This setting allows the specified IRQ to be used by a PCI/PnP device.
	Reserved	This setting allows the specified IRQ to be used by a legacy ISA device.

DMA Channel 0 - DMA Channel 7

Available: Specified DMA is available to be used by PCI/PnP devices.
Reserved: Specified DMA is reserved for use by Legacy ISA devices.

DMA	Option	Description
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	Available (Default)	This setting allows the specified DMA to be used by a PCI/PnP device.
	Reserved	This setting allows the specified DMA to be used by a legacy ISA device.

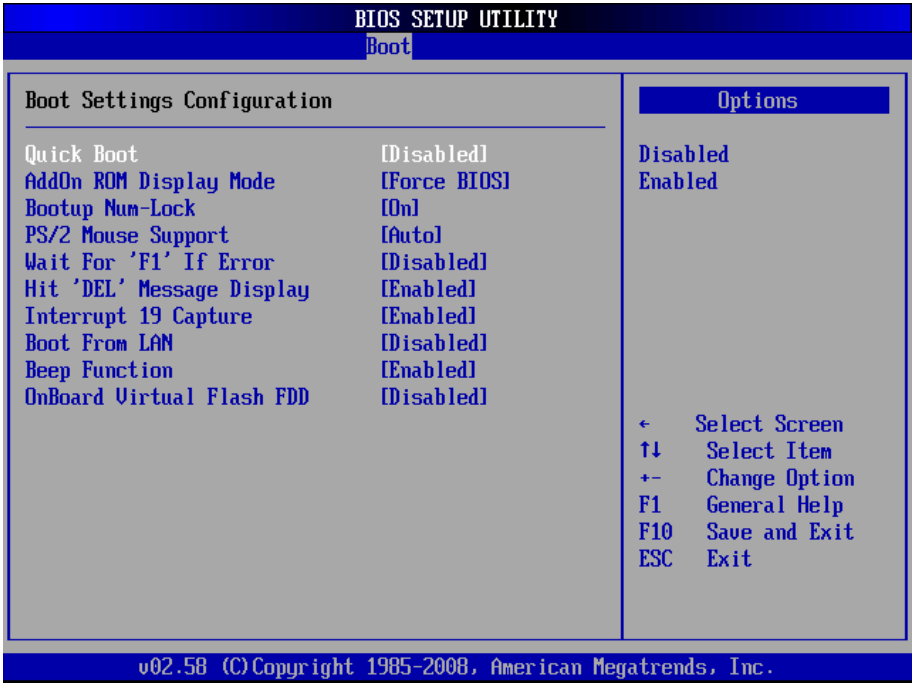
Reserved Memory Size

Set this value to allow the system to reserve memory that is used by ISA device.

Option	Description
Disabled (Default)	Set this value to prevent BIOS from reserving memory to ISA devices.
16K	Set this value to allow the system to reserve 16K of the system memory to the ISA devices.
32K	Set this value to allow the system to reserve 32K of the system memory to the ISA devices.
64K	Set this value to allow the system to reserve 64K of the system memory to the ISA devices.

3.4 Boot Settings

The Boot menu items allow you to change the system boot options. Select an item then press <Enter> to display the sub-menu.



Quick Boot

Set the value to Enabled to allow the BIOS to skip some Power On Self Tests (POST) while booting to decrease the time needed to boot the system. When you set the value to Disable the BIOS will performs all the POST items.

Option	Description
Disabled	Set this value to allow the BIOS to perform all POST tests.
Enabled (Default)	Set this value to allow the BIOS to skip certain POST tests to boot faster.

AddOn ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The Optimal and Fail-Safe default setting is Force BIOS. An example of this is a SCSI BIOS or VGA BIOS.

Option	Description
Force BIOS (Default)	Set this value to allow the computer system to force a third party BIOS to display during system boot.
Keep Current	Set this value to allow the computer system to display the ezPORT information during system boot.

Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. The
Optimal and Fail-Safe default setting is On.

Option	Description
Off	This option does not enable the keyboard Number Lock automatically. To use the 10-key on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard will light up when the Number Lock is engaged.
On (Default)	Set this value to allow the Number Lock on the keyboard to be enabled automatically when the computer system is boot up. This allows the immediate use of 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard will be lit.

PS/2 Mouse Support

Set this value to allow the PS/2 mouse support to be adjusted. The Optimal and Fail-Safe default setting is Enabled.

Option	Description
Disabled	This option will prevent the PS/2 mouse port from using system resources and will prevent the port from being active. Use this setting if installing a serial mouse.
Enabled (Default)	Set this value to allow the system to use a PS/2 mouse.

Wait For “F1” If Error

Set this value to allow the Wait for <F1> Error setting to be modified. The Optimal and Fail-Safe default setting is Enabled

Option	Description
Disabled	This prevents the ezPORT to wait on an error for user intervention. This setting should be used if there is a known reason for a BIOS error to appear. An example would be a system administrator must remote boot the system. The computer system does not have a keyboard currently attached. If this setting is set, the system will continue to boot up in to the operating system. If <F1> is enabled, the system will wait until the BIOS setup is entered.
Enabled (Default)	Set this value to allow the system BIOS to wait for any error. If an error is detected, pressing <F1> will enter Setup and BIOS setting can be adjusted to fix the problem. This normally happens when upgrading the hardware and not setting the BIOS to recognize it.

Hit “DEL” Massage Display

Set this value to allow the Hit “DEL” to enter Setup Message Display to be modified.
The Optimal and Fail-Safe default setting is Enabled.

Option	Description
Disabled	This prevents the ezPORT to display “Hit Del to enter Setup” during memory initialization. If Quiet Boot is enabled, the Hit "DEL" message will not display.
Enabled (Default)	This allows the ezPORT to display “Hit Del to enter Setup” during memory initialization.

Interrup 19 Capture

Set this value to allow option ROMs such as network controllers to trap BIOS interrupt 19.

Option	Description
Disabled (Default)	The BIOS prevents option ROMs from trapping interrupt 19.
Enabled	The BIOS allows option ROMs to trapping interrupt 19.

Boot From LAN

This allows you to select the value of the LAN boot Function.

Beep Function

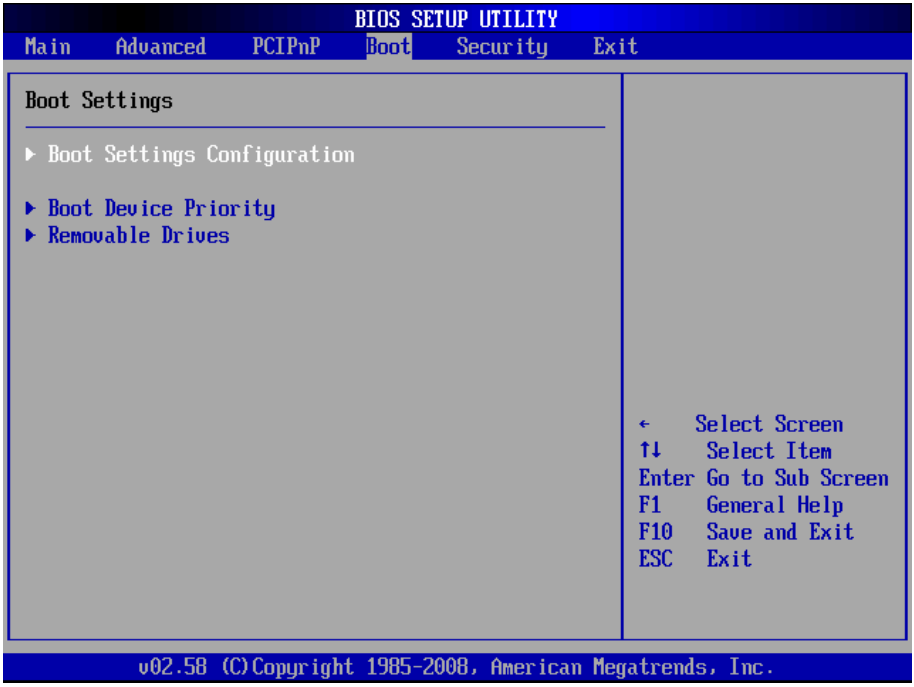
Set this value to allow the system to enable or disable generating a beep during posting success.

OnBoard Virtual Flash FDD

This allows you to “Enable” or “Disable” the onboard SPI FLASH-DISK.

3.4.1 Boot Device Priority

Use this screen to specify the order in which the system checks for the device to boot from. To access this screen, select Boot Device Priority on the Boot Setup screen and press <Enter>.



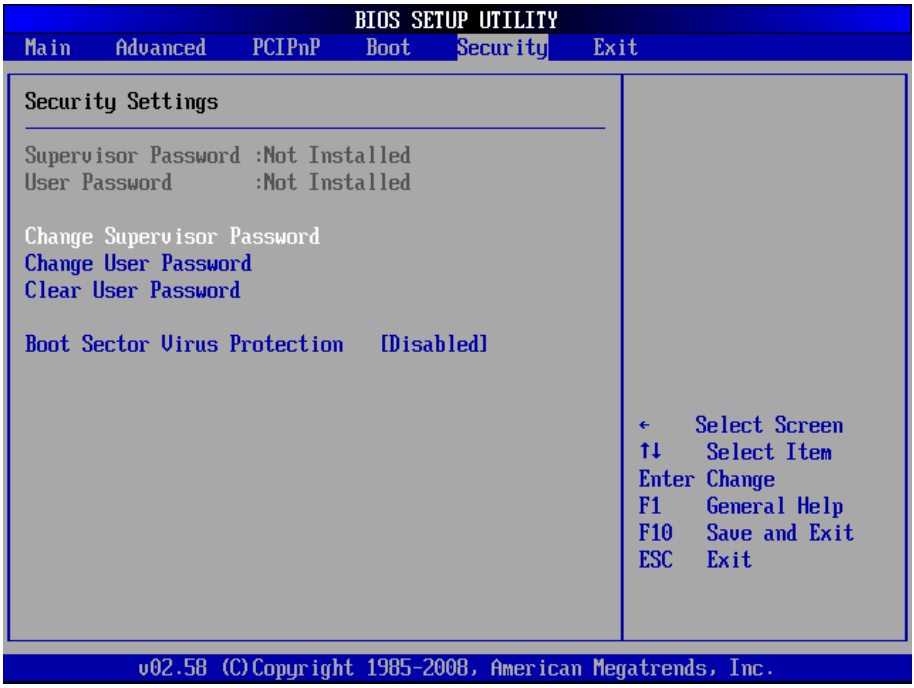
Boot Device Priority

Press Enter and it shows Bootable add-in devices.

Removable Drives

Press Enter and it shows Bootable and Removable drives.

3.5 Security



Supervisor Password & User Password

You can set either supervisor or user password, or both of then. The differences between are:

Set ***Supervisor Password***: Can enter and change the options of the setup menus.

Set ***User Password***: Just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

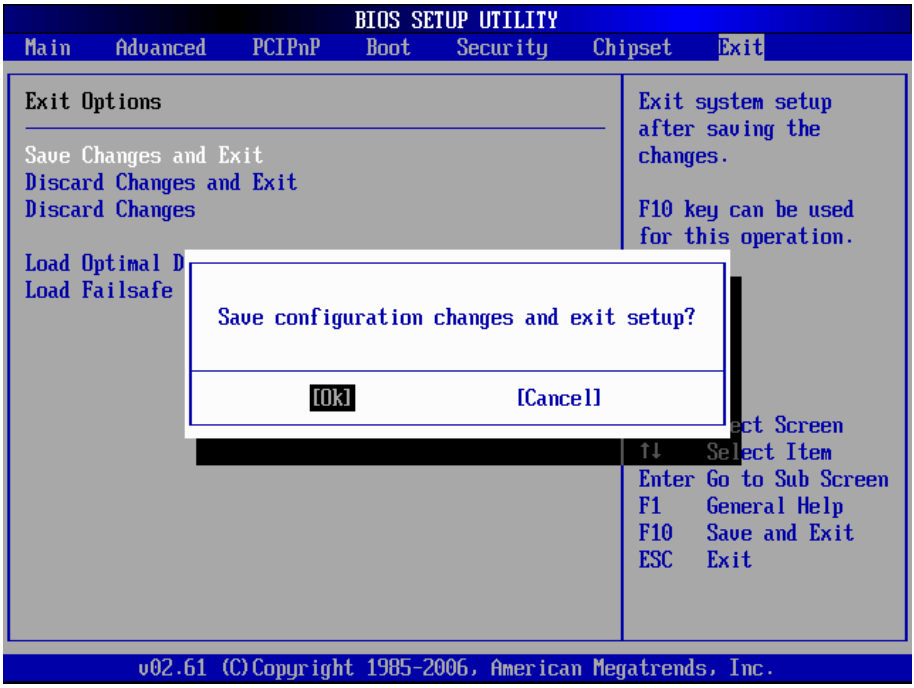
Boot Sector Virus Protection

This option is near the bottom of the Security Setup screen. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled (Default)	Set this value to prevent the Boot Sector Virus Protection.
Enabled	Select Enabled to enable boot sector protection ezPORT displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write.

3.6 Exit Options

Save Changes and Exit



Pressing <Enter> on this item asks for confirmation:

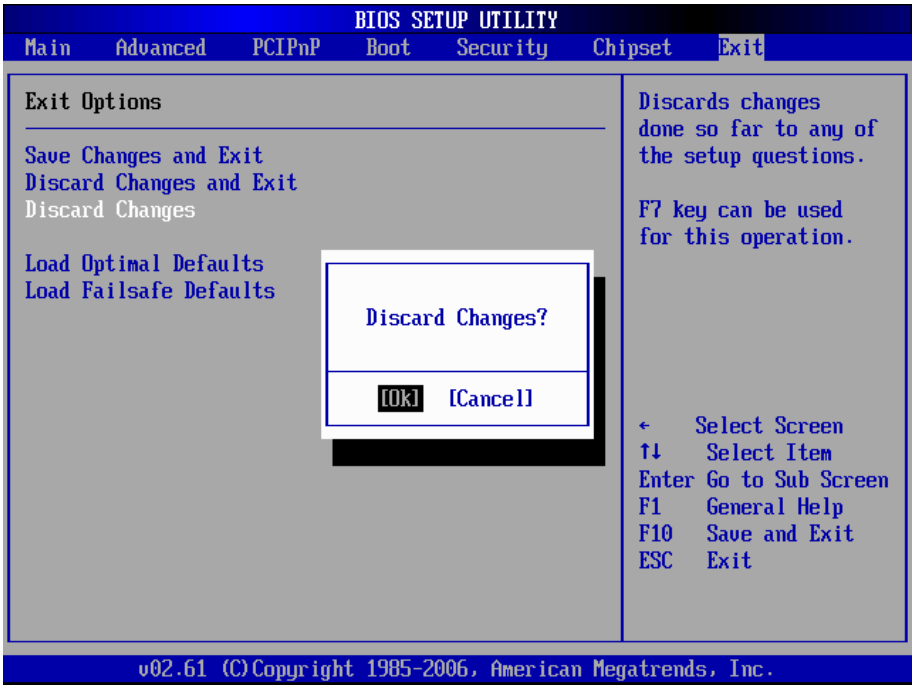
Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit

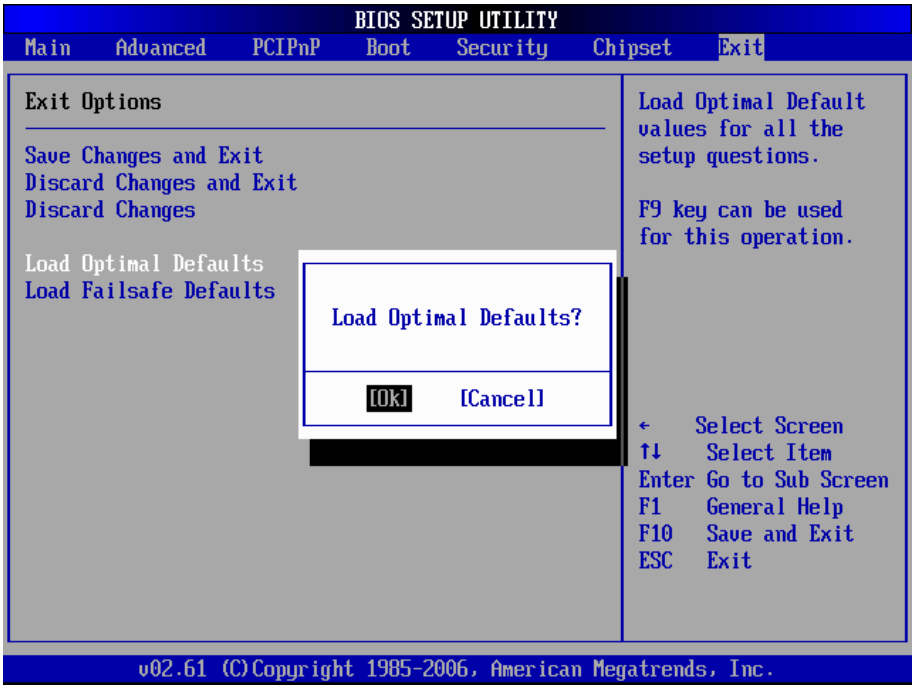
Exit system setup without saving any changes.
<ESC> key can be used for this operation.

Discard Changes


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Discard Changes?
[Ok] [Cancel]
Discards changes done so far to any of the setup questions.
F7 key can be used for this operation.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

Discards changes done so far to any of the setup questions.
<F7> can be used for this operation.

Load Optimal Defaults


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Load Optimal Defaults?
[Ok] [Cancel]
Load Optimal Default values for all the setup questions.
F9 key can be used for this operation.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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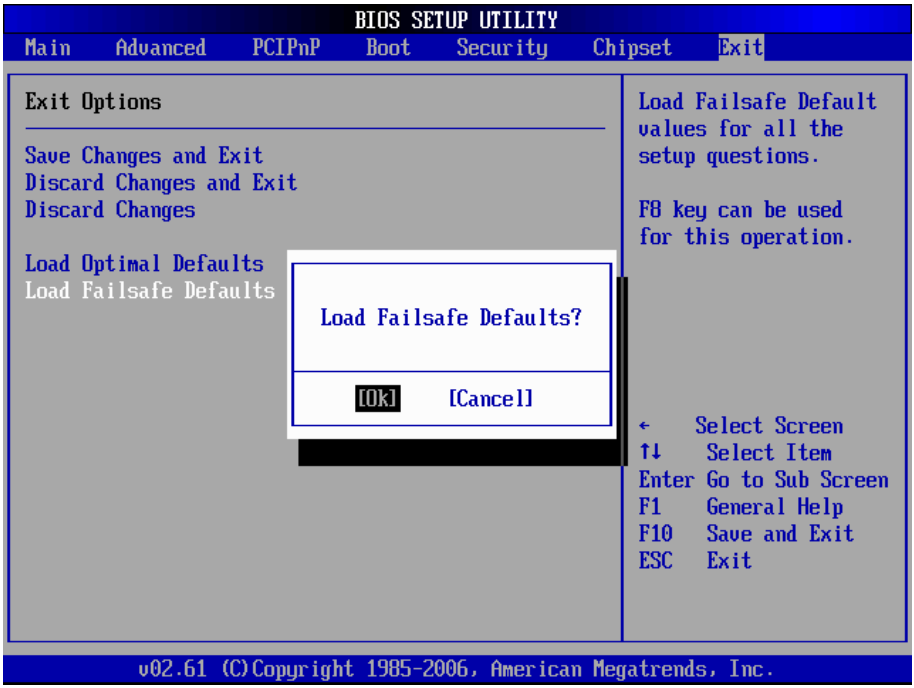
When you press <Enter> on this item you get a confirmation dialog box with a message:

Load Optimal Defaults?
[OK] [Cancel]

Pressing [OK] loads the BIOS Optimal Default values for all the setup questions.

<F9> key can be used for this operation.

Load Failsafe Defaults


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Load Failsafe Default values for all the setup questions.
F8 key can be used for this operation.
Load Failsafe Defaults?
[Ok] [Cancel]
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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When you press <Enter> on this item you get a confirmation dialog box with a message:

Load Failsafe Defaults?
[OK] [Cancel]

Pressing [OK] loads the BIOS Failsafe Default values for all the setup questions.

<F8> key can be used for this operation.

3.7 Beep Sound codes list

3.7.1 Boot Block Beep Codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.7.2 POST BIOS Beep Codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.7.3 Troubleshooting POST BIOS Beep Codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem
8	If the system video adapter is an add-in card, replace or reset the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.8 AMI BIOS Checkpoints

3.8.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processo (BSP) initialization like microcode update, frequency and other CPU cirtical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is deisabled. Perfrom keyboard controller BAT test. Save power-on CPUID value in scretch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perfroms main BIOS checksum and updates recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows tocheckpoint E0. Seed *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether in memory.
D8	The Tuntime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is saking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to be next.

3.8.2 Bootclock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to red from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.8.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.

38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to theuser and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupt by invoking all handlers.
A1	Lian-up work needed before booting to OS.

A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for userinput at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

3.8.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

Chapter 5

Appendix

4.1 I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0000h-0000Fh 0080h-009Fh 00C0h-00DFh	DMA Controller
0020h , 0021h 00A0h , 00A1h	Programmable interrupt Controller
0040h-0043h 0044h-0047h	System timer
0060h-0064h	Keyboard controller
0070h-0071h	System CMOS/real time clock
00F0h-00FFh	Math Co-Processor
01F0h-01F7h	Primary IDE
0274h-0277h	ISAPNP Read Data Port
0279h , 0A79h	ISAPnP Configuration
02E8h-02EFh	COM_4 (If use)
02F8h-02FFh	COM_2 (If use)
0378h-037Ah	Parallel Port (If use)
03B0h-03BFh	MDA/MGA
03C0h-03CFh	EGA/VGA
03D4h-03D9h	CGA CRT Register
03F0h-03F7h	Floppy Diskette (If use)
03F8h-03FFh	COM_1 (If use)
0400h-041F	South Bridge SMB
04D0h-04D1h	IRQ Edge/level control ports
0500h-053Fh	South Bridge GPIO
0800h-087Fh	ACPI
0A00h-0A07h	PME
0CF8h	PCI Configuration address
0CFCh	PCI Configuration Data

4.2 Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 00	System Timer
IRQ 01	Keyboard Controller
IRQ 02	VGA and Link to Secondary PIC
IRQ 03	Communications Port 2
IRQ 04	Communications Port 1
IRQ 05	PCI Device
IRQ 06	Floppy Controller
IRQ 07	Parallel Port
IRQ 08	CMOS/ RTC Timer
IRQ 09	ACPI
IRQ 10	Communications Port 3
IRQ 11	Communications Port 4
IRQ 12	PS/2 Mouse
IRQ 13	FPU exception
IRQ 14	IDE Controller
IRQ 15	PCI Device

4.3 Memory Address Map

Address	Device Description
00000h-9FFFFh	DOS Kernel Area
A0000h,BFFFFh	EGA and VGA Video Buffer (128KB)
C0000h-CFFFFh	EGA/VGA ROM
D0000h-DFFFFh	Adapter ROM
E0000h-FFFFFh	System BIOS

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